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# Claims

[c1] A solder interconnect used with an integrated circuit structure, said interconnect comprising:
a metal layer on a substrate;
a first copper layer on said metal layer;
a barrier layer on said copper layer;
a stabilizing copper layer on said barrier layer; and
a tin-based solder bump on said barrier layer.

[c2] The interconnect in claim 1, wherein said stabilizing copper layer comprises a sufficient amount of copper to balance the chemical potential gradient of copper across said barrier layer and prevent copper within said first copper layer from diffusing across said barrier layer.

[c3] The interconnect in claim 1, wherein said tin-based solder bump comprises a copper rich solder alloy.

[c4] The interconnect in claim 1, wherein said metal layer comprises diffusion metallurgy including at least one of Al, Ti, TiW, Cr, Ta, and TaN.

[c5] The interconnect in claim 1, wherein said barrier layer comprises one of Ni, V, and NiV.

[c6] The interconnect in claim 1, wherein said tin-based solder bump comprises one of a eutectic PbSn solder and lead-free solders.

[c7] A solder interconnect used with an integrated circuit structure, said interconnect comprising:
a metal layer on a substrate;
a first copper layer on said metal layer;
a barrier layer on said copper layer;
a copper and tin-based solder alloy bump on said barrier layer.

[c8] The interconnect in claim 7, wherein said copper and tin-based solder alloy bump comprises a sufficient amount of copper to balance the chemical potential gradient of copper across said barrier layer and prevent copper within said first copper layer from diffusing across said barrier layer.

[c9] The interconnect in claim 7, wherein said metal layer comprises diffusion metallurgy including at least one of Al, Ti, TiW, Cr, Ta, and TaN.

[c10] The interconnect in claim 7, wherein said barrier layer comprises one of Ni, V, and NiV.

[c11] The interconnect in claim 7, wherein said tin-based solder alloy bump comprises one of a eutectic PbSn solder

and lead-free solders.

[c12] An integrated circuit structure comprising:
internal circuitry; and
an interconnect on an external portion of said structure,
said interconnect comprising:
a metal layer on said external portion of said structure;
a first copper layer on said metal layer;
a barrier layer on said copper layer;
a stabilizing copper layer on said barrier layer; and
a tin-based solder bump on said barrier layer.

[c13] The structure in claim 12, wherein said stabilizing copper layer comprises a sufficient amount of copper to balance the chemical potential gradient of copper across said barrier layer and prevent copper within said first copper layer from diffusing across said barrier layer.

[c14] The structure in claim 12, wherein said tin-based solder bump comprises a copper rich solder alloy.

[c15] The structure in claim 12, wherein said metal layer comprises diffusion metallurgy including at least one of Al, Ti, TiW, Cr, Ta, and TaN.

[c16] The structure in claim 12, wherein said barrier layer comprises one of Ni, V, and NiV.

[c17] The structure in claim 12, wherein said tin-based solder bump comprises one of a eutectic PbSn solder and lead-free solders.

[c18] An integrated circuit structure comprising:
internal circuitry; and
an interconnect on an external portion of said structure, said interconnect comprising:
a metal layer on said external portion of said structure;
a first copper layer on said metal layer;
a barrier layer on said copper layer;
a copper and tin-based solder alloy bump on said barrier layer.

[c19] The structure in claim 18, wherein said copper and tin-based solder alloy bump comprises a sufficient amount of copper to balance the chemical potential gradient of copper across said barrier layer and prevent copper within said first copper layer from diffusing across said barrier layer.

[c20] The structure in claim 18, wherein said metal layer comprises diffusion metallurgy including at least one of Al, Ti, TiW, Cr, Ta, and TaN.

[c21] The structure in claim 18, wherein said barrier layer comprises one of Ni, V, and NiV.

[c22] The structure in claim 18, wherein said tin-based solder alloy bump comprises one of a eutectic PbSn solder and lead-free solders.